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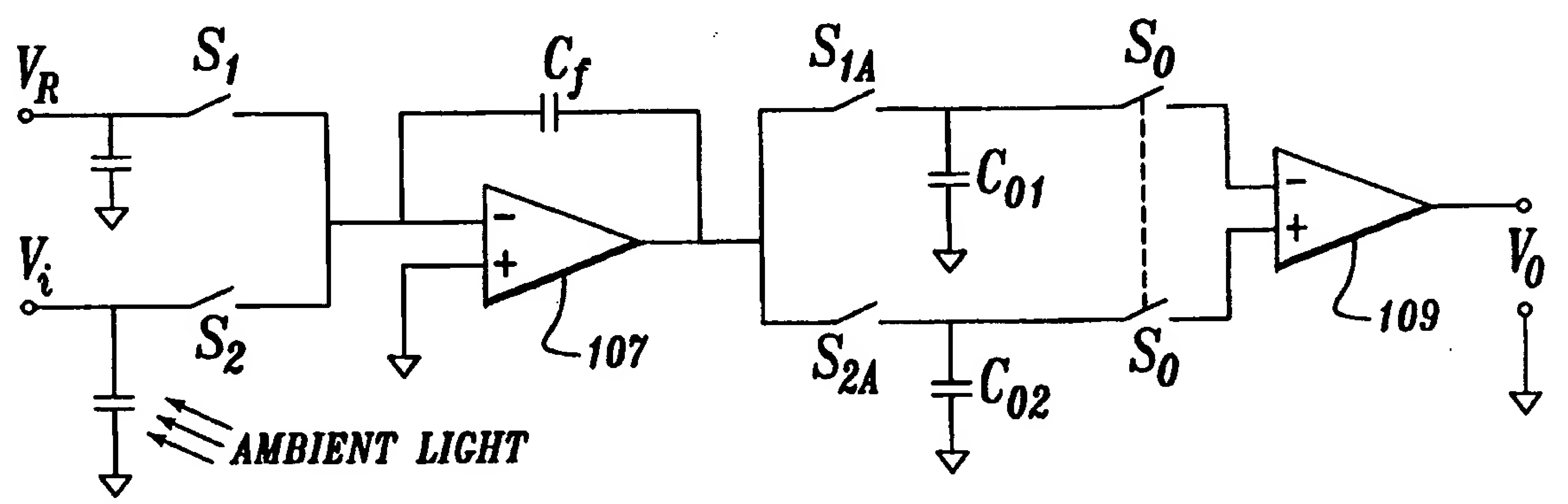
(54) Title: IMPROVED CHARGE AMPLIFIER FOR MOS IMAGING ARRAY



(57) Abstract

An improved charge amplifier (105) for use in a MOS imaging array is disclosed. The charge amplifier comprises a reference capacitor (C_r), a sense capacitor (C_s), an operational amplifier (107), a first output capacitor (C_{o1}) connected to the output of the operational amplifier, a second output capacitor (C_{o2}) connected to the output of the operational amplifier, and a differential amplifier (109) connected to the first output capacitor and said second output capacitor. In operation, the reference capacitor is charged to a reference voltage. Similarly, the sense capacitor is charged to a reference voltage. Both the sense capacitor and the reference capacitor are formed to be identical. However, the reference capacitor is covered from ambient light and the sense capacitor is exposed to ambient light. As ambient light is incident on the sense capacitor, the voltage carried by the sense capacitor diminishes. After a predetermined exposure time, both the voltage stored across the reference capacitor and the sense capacitor is amplified by the operational amplifier. Next, the differential amplifier operates to provide an output signal that is the difference between said amplified version of said reference voltage and said amplified version of said signal voltage.

IMPROVED CHARGE AMPLIFIER FOR MOS IMAGING ARRAY

Related Applications

This is a continuation-in-part of pending U.S. patent application Ser. No. 08/617,313 filed March 18, 1996, which is a continuation-in-part of pending U.S. patent application Ser. No. 08/538,441 filed October 3, 1995.

Field of the Invention

The present invention relates to metal oxide semiconductor imaging arrays, and more particularly, an improved charge amplifier for use in the array.

Background of the Invention

Integrated circuit technology has revolutionized various fields including computers, control systems, telecommunications, and imaging. In the field of imaging, the charge coupled device (CCD) sensor has made possible the manufacture of relatively low cost and small hand-held video cameras. Nevertheless, the solid-state CCD integrated circuits needed for imaging are relatively difficult to manufacture, and therefore are expensive. In addition, because of the differing processes involved in the manufacture of CCD integrated circuits relative to MOS integrated circuits, the signal processing portion of the imaging sensor has typically been located on a separate integrated chip. Thus, a CCD imaging device includes at least two integrated circuits: one for the CCD sensor and one for the signal processing logic.

An alternative low cost technology to CCD integrated circuits is the metal oxide semiconductor (MOS) integrated circuit. Not only are imaging devices using MOS technology less expensive to manufacture relative the CCD imaging devices, for certain applications MOS devices are superior in performance. For example, the pixel

elements in a MOS device can be made smaller and therefore provide a higher resolution than CCD image sensors. In addition, the signal processing logic necessary can be integrated alongside the imaging circuitry, thus allowing for a single integrated chip to form a complete stand alone imaging device.

Examples of MOS imaging devices are detailed in "A ¼ Inch Format 250K Pixel Amplified MOS Image Sensor Using CMOS Process" by Kawashima et al., *IEDM* 93-575 (1993), and "A Low Noise Line-Amplified MOS Imaging Devices" by Ozaki et al., *IEEE Transactions on Electron Devices*, Vol. 38, No. 5, May 1991. In addition, U.S. Patent No. 5,345,266 to Denyer titled "Matrix Array Image Sensor Chip" describes a MOS image sensor. The devices disclosed in these publications provide a general design approach to MOS imaging devices.

The primary building block of an image formed by an MOS imaging device is a pixel. The number, size and spacing of the pixels determine the resolution of the image generated by the imaging device. The pixels of a MOS imaging device are semiconductor devices that transform incident light photons into current signals. The signal produced by each pixel is generally extremely small, in the nanoampere range. This small signal is unsuitable for further processing. Thus, a critical component of a MOS image sensor is a series of charge amplifiers that amplify the signals generated by the pixel elements. It is the charge amplifier design that is the subject of the present invention.

Summary of the Invention

An improved charge amplifier for use in a MOS imaging array is disclosed. The charge amplifier comprises a reference capacitor, a sense capacitor, an operational amplifier, a first output capacitor connected to the output of the operational amplifier, a second output capacitor connected to the output of the operational amplifier, and a differential amplifier connected to the first output capacitor and said second output capacitor.

In operation, the reference capacitor is charged to a reference voltage. Similarly, the sense capacitor is charged to a reference voltage. Both the sense capacitor and the reference capacitor are formed to be identical. However, the reference capacitor is covered from ambient light and the sense capacitor is exposed to ambient light. As ambient light is incident on the sense capacitor, the voltage carried by the sense capacitor diminishes. After a predetermined exposure time, both the voltage stored across the reference capacitor and the sense capacitor is amplified by the operational amplifier. Next, the differential amplifier operates to provide an

output signal that is the difference between said amplified version of said reference voltage and said amplified version of said signal voltage.

Brief Description of the Drawings

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIGURE 1A is a schematic diagram of a CMOS imaging sensor;

FIGURE 1B is a schematic diagram of a CMOS charge amplifier formed in accordance with the present invention;

FIGURES 2A-2E are timing diagrams illustrating the operation of the CMOS charge amplifier of FIGURE 1A;

FIGURE 3 is a circuit diagram illustrating the charge amplifier of FIGURE 1A during a third time period;

FIGURE 4 is a circuit diagram illustrating the charge amplifier of FIGURE 1A during a fourth time period; and

FIGURE 5 is a circuit diagram illustrating the charge amplifier of FIGURE 1A during a fifth time period.

Detailed Description of the Preferred Embodiment

With reference to FIGURE 1A, a CMOS imaging array 101 in accordance with the present invention includes a rectangular matrix of pixels 103. The number of pixels in the horizontal or x-direction, and the number of pixels in the vertical or y-direction, constitutes the resolution of the imaging array 101. Each of the pixels 103 in a vertical column routes its signal to a single charge amplifier 105 (shown in greater detail in FIGURE 1B). However, at any instant only one of the pixels 105 in a column sends a charge signal to the associated charge amplifier 105. Control circuitry of conventional design is operative to sequentially read the pixels 103 in a scanning manner.

As seen in FIGURE 1B, each charge amplifier 105 of the present invention (also referred to in the art as a sense amplifier) includes a sense capacitor C_s, a reference capacitor C_r, an operational amplifier 107, a feedback capacitor C_f, a first output capacitor C_{01}, a second output capacitor C_{02}, a differential amplifier 109, and switches S_0, S_1, S_2, S_{1a}, and S_{2a}.

A feedback capacitor C_F is connected between the negative input and the output of the operational amplifier 107. In the preferred embodiment, the capacitors are formed by MOS devices. As described below, switches S_0, S_1, S_2, S_{1a}, and S_{2a}

control the routing of the input signal (V_i), reference voltage signal (V_{REF}) and feedback signal through the amplifier.

The reference capacitor C_r is connected between ground and the inverting input of operation amplified 107. Between the reference capacitor C_r and the inverting input to the operational amplifier 107 is switch S_1.

The sense capacitor C_S is also connected between ground and the inverting input of the operational amplifier 107. Switch S_2 is placed between the sense capacitor C_S and the inverting input to operational amplifier 107. Sense capacitor C_S also stores the input signal V_i. Indeed, the sense capacitor C_S is the sensing element used to determine the amount of ambient light incident on that particular pixel.

The non-inverting input of operational amplifier 107 is connected to ground. Alternatively, the non-inverting input of operational amplifier 107 may be connected to a second voltage reference. As noted above, the output of the operational amplifier 107 is fed back into the inverting input of the operational amplifier 107 through feedback capacitor C_f.

The output of operational amplifier 107 is provided via switch S_{1a} to an input terminal of first output capacitor C_{o1}. The other terminal of the first output capacitor C_{o1} is connected to ground. As seen in FIGURE 1B, also connected to the input terminal of the first output capacitor C_{o1} is switch S_0 that leads to the inverting input of differential amplifier 109.

The output of operational amplifier 107 is also provided via switch S_{2a} to an input terminal of second output capacitor C_{o2}. The other terminal of the second output capacitor C_{o2} is connected to ground. As seen in FIGURE 1B, also connected to the input terminal of the second output capacitor C_{o2} is switch S_o that leads to the non-inverting input of differential amplifier 109.

Finally, the output of differential amplifier 109 provides the output signal V_o.

The operation of the charge amplifier 105 of FIGURE 1B can be seen in greater detail with reference to the timing diagram of FIGURE 2. During a first time period, t_1; switch S_2 is closed and the sense capacitor C_S is charged to a reference voltage V_r. All of the other switches are open at this point. However, because the sense capacitor is exposed to ambient light, the voltage initially stored in sense capacitor C_s (V_r) begins to decline as the ambient light strikes the sense capacitor C_s. Sense capacitors C_s that behave in this manner are known in the art. Thus, the voltage across sense capacitor C_s begins to decline from V_r to a value V_i as ambient light strikes the sense capacitor C_s. As will be seen in further detail below, the voltage V_i will be reached at the beginning of a fourth time period t_4 when the signal

carried across the sense capacitor C_s is amplified. The time period from the charging of the sense capacitor C_s until the beginning of the fourth time period t_4 is referred to as the "exposure time" because that is how long the sense capacitor C_s will be exposed to the ambient light before the V_i signal is amplified.

Next, during a second period, t_2, switch S1 is closed and the reference capacitor C_r is charged to the reference voltage V_r. All of the other switches are open at this point. Thus, both the sense capacitor C_s and the reference capacitor C_r are initially charged to the same reference voltage V_r. Because the reference capacitor C_r is not exposed to ambient light, its voltage stays constant at V_r.

Next, at a third time period, t_3, switches S_1 and S_{1a} are closed while all of the remaining switches are opened. The resulting circuit is shown in FIGURE 3. During this third time period, the first output capacitor C_{o1} carries an amplified version of the signal V_r stored by reference capacitor C_r. It can be appreciated that under the circuit shown in FIGURE 3, the voltage stored across first output capacitor C_{o1} is equal to the voltage stored across reference capacitor C_r, V_r, multiplied by the ratio of C_r/C_f. Thus, the first output capacitor C_{o1} stores a "baseline voltage" of V_r amplified by the operational amplifier 107. The baseline voltage indicates the voltage output from a pixel that has no ambient incident light.

Next, at a fourth time period, t_4, switches S_2 and S_{2a} are closed. The resultant circuit is shown in FIGURE 4. Similar to the situation as described with reference to FIGURE 3, the second output capacitor C_{o2} carries the charge across the sense capacitor C_S , V_i, amplified by a factor of C_S/C_f. Therefore, the second output capacitor C_{o2} contains the amplified version of V_i.

At this juncture, the first output capacitor C_{o1} contains an amplified version of the signal carried by reference capacitor C_r. Similarly, the second output capacitor C_{o2} will carry an amplified version of the signal carried by sense capacitor C_S. The voltage across the second capacitor C_{o2} will usually be greater than that across the first capacitor C_{o1} because the voltage V_i will typically be less than the voltage V_r.

Finally, during a fifth time period, t_5, all switches are opened except for the pair of switches S_0. This allows the signals that are carried in the first and second output capacitors C_{o1} and C_{o2} to be input into differential amplifier 109. An equivalent circuit is shown in FIGURE 5. The differential amplifier 109 serves, in a manner well known in the art, to provide an output that is the difference between its inverting and non-inverting inputs. This differential amplifier 109 provides an output that is the final output voltage V_o. The output voltage V_o then indicates the amount

of light incident upon the sense capacitor C_s during the exposure time. The higher the value of V_0 the higher the amount of incident light on the sense capacitor C_s during the exposure time. It should be noted that the sense capacitor C_S and the reference capacitor C_r are formed from exactly the identical dimensions and are identical in every way.

Further, in the preferred embodiment, the first and second time periods are 3480 nanoseconds, the fifth time period is 174 nanoseconds, and the third and fourth time periods t_3 and t_4 are 1044 nanoseconds.

While the preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changes can be made therein without departing from the spirit and scope of the invention.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A method of amplifying an ambient light signal from a pixel in a MOS imaging array, said pixel including a sensing element, the method comprising the steps of:

generating a reference voltage signal onto a reference element formed substantially identical to said sensing element, said reference element shielded from ambient light;

generating an ambient light signal by generating said reference voltage signal onto said sensing element and decreasing said reference voltage signal in a deterministic manner in response to incident ambient light;

amplifying said reference voltage signal to generate an amplified reference voltage signal;

amplifying said ambient light signal to generate an amplified ambient light signal; and

generating an output signal as the difference between said amplified reference voltage signal and said amplified ambient light signal.

2. The method of Claim 1 further including the step of amplifying said difference between said amplified reference voltage signal and said amplified ambient light signal.

3. The method of Claim 1 further including the steps of:

storing said amplified reference voltage signal in a first storage capacitor;

storing said amplified ambient light signal in a second storage capacitor; and

providing said amplified reference voltage signal and said amplified ambient light signal to a differential amplifier for amplification.

4. A method of amplifying an ambient light signal generated by a pixel in a MOS imaging array, said pixel including a sensing element, the method comprising the steps of:

generating a reference voltage signal onto a reference element formed substantially identically to said sensing element;

generating said ambient light signal by exposing said sensing element to ambient light;

amplifying said reference voltage signal and said ambient light signal; and

calculating the difference between said reference voltage signal and said ambient light signal.

5. The method of Claim 4 wherein said step of generating said ambient light signal includes the steps of:

generating onto said sensing element said reference voltage;

exposing said sensing element to said ambient light, said ambient light causing said sensing element to deterministically decrease said reference voltage signal to said ambient light signal.

6. The method of Claim 4 further including the step of amplifying said difference between said reference voltage signal and said ambient light signal.

7. The method of Claim 5 further including the step of amplifying said difference between said reference voltage signal and said ambient light signal.

8. The method of Claim 4 further including the steps of:

storing said amplified reference voltage signal in a first storage capacitor;

storing said amplified ambient light signal in a second storage capacitor; and

providing said amplified reference signal and said amplified ambient light signal to a differential amplifier for amplification.

9. The method of Claim 5 further including the steps of:

storing said amplified reference voltage signal in a first storage capacitor;

storing said amplified ambient light signal in a second storage capacitor; and

providing said amplified reference signal and said amplified ambient light signal to a differential amplifier for amplification.

10. The method of Claim 6 further including the steps of:

storing said amplified reference voltage signal in a first storage capacitor;

storing said amplified ambient light signal in a second storage capacitor; and

providing said amplified reference signal and said amplified ambient light signal to a differential amplifier for amplification.

11. An improved charge amplifier for use in a MOS imaging array, said charge amplifier comprising:

an operational amplifier having an inverting input and an amplifier output terminal for outputting an amplifier signal;

a feedback capacitor connected between said inverting input and said amplifier output terminal;

a reference capacitor for storing a reference voltage, said reference capacitor connected to said inverting input;

a sense capacitor for carrying said signal voltage, said sense capacitor connected to said inverting input;

a first output capacitor connected to said amplifier output terminal and for storing an amplified version of said reference voltage;

a second output capacitor connected to said amplifier output terminal and for storing an amplified version of said signal voltage; and

a differential amplifier connected to said first output capacitor and said second output capacitor, said differential amplifier providing an output signal that is the difference between said amplified version of said reference voltage and said amplified version of said signal voltage.

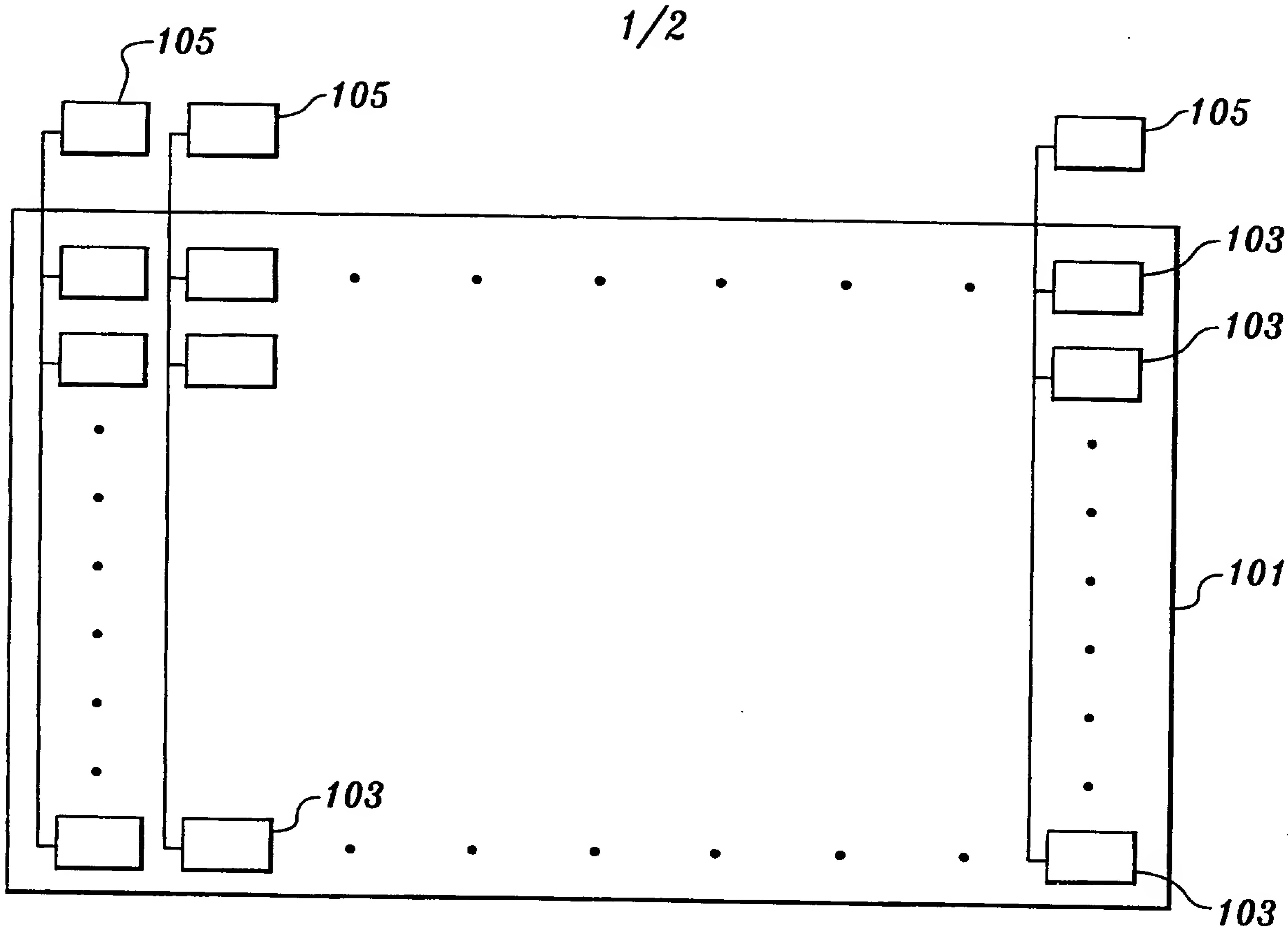

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Fig. 1A

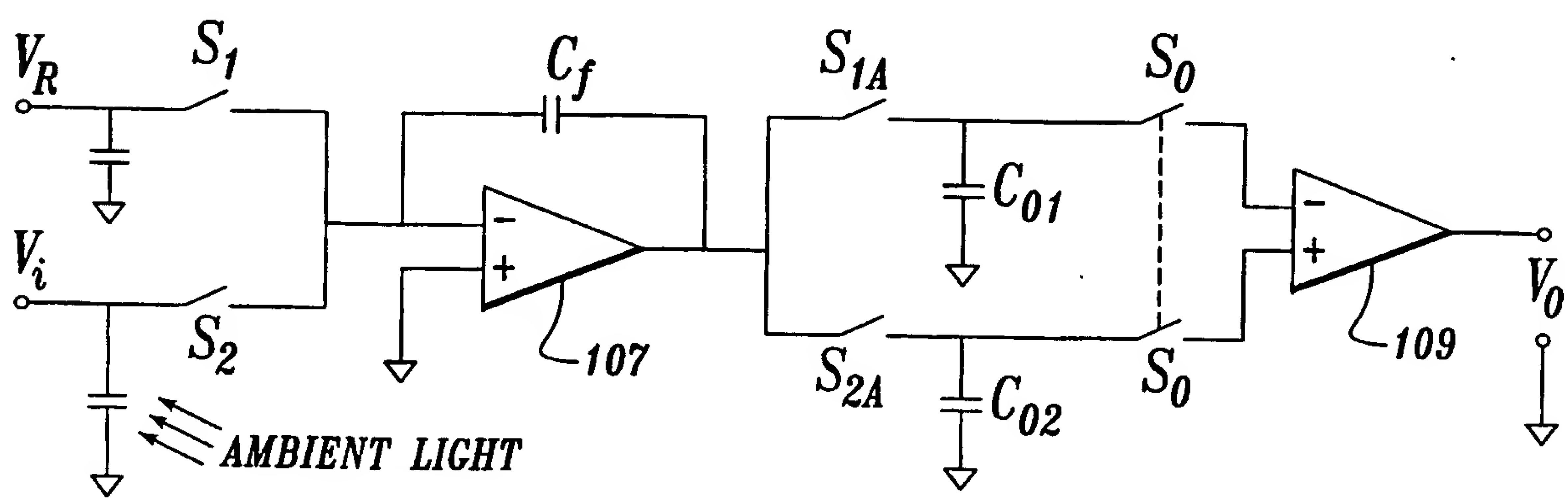

V_R
S_1
C_f
S_{1A}
S_0
C_{01}
V_i
S_2
107
S_{2A}
C_{02}
S_0
109
V_0
AMBIENT LIGHT

Fig. 1B

Fig. 2A

Fig. 2B

Fig. 2C

Fig. 2D

Fig. 2E

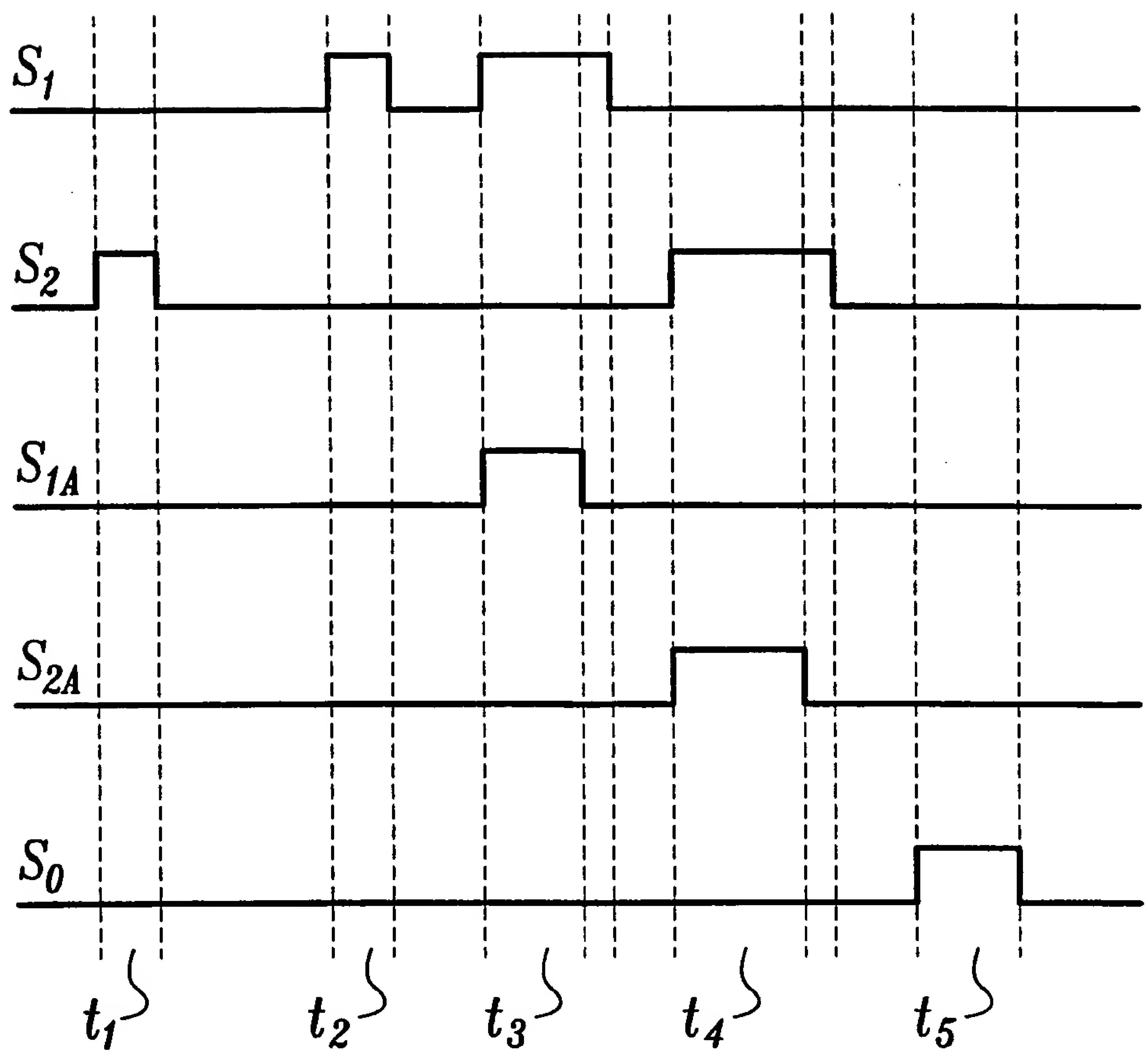


Fig. 3

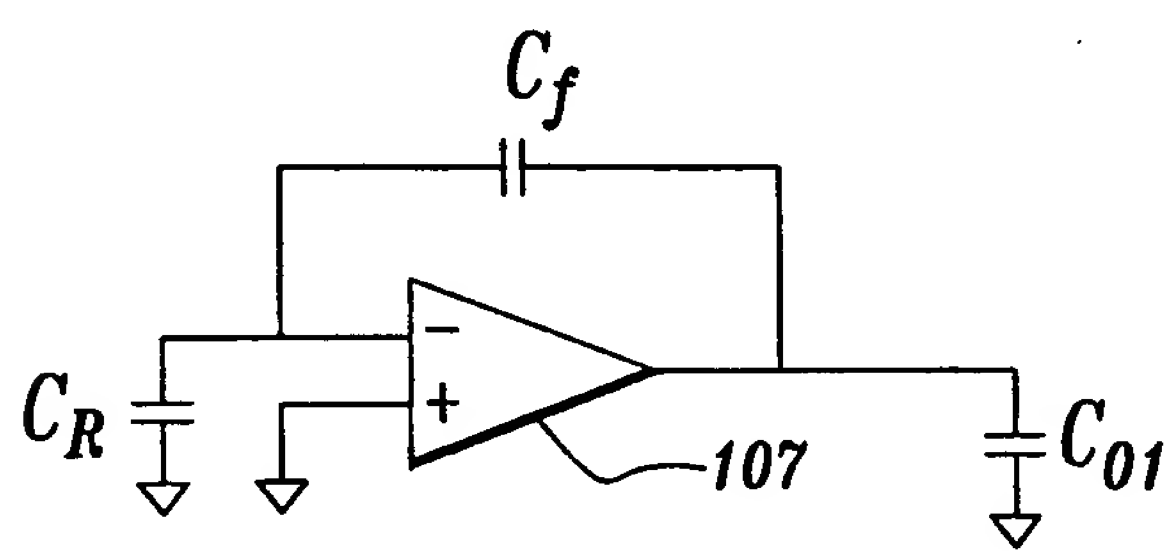


Fig. 4

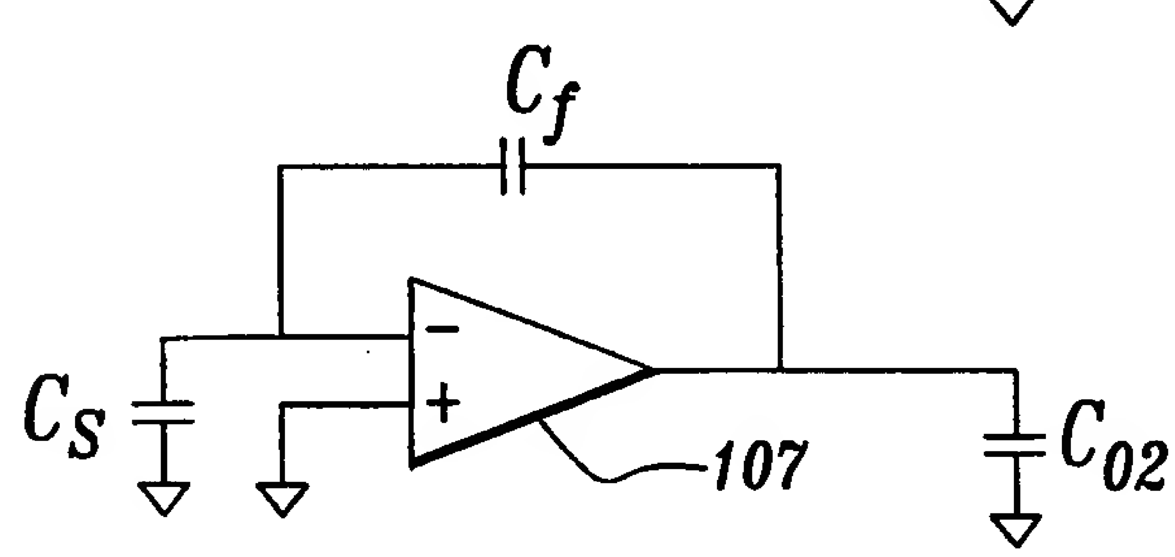
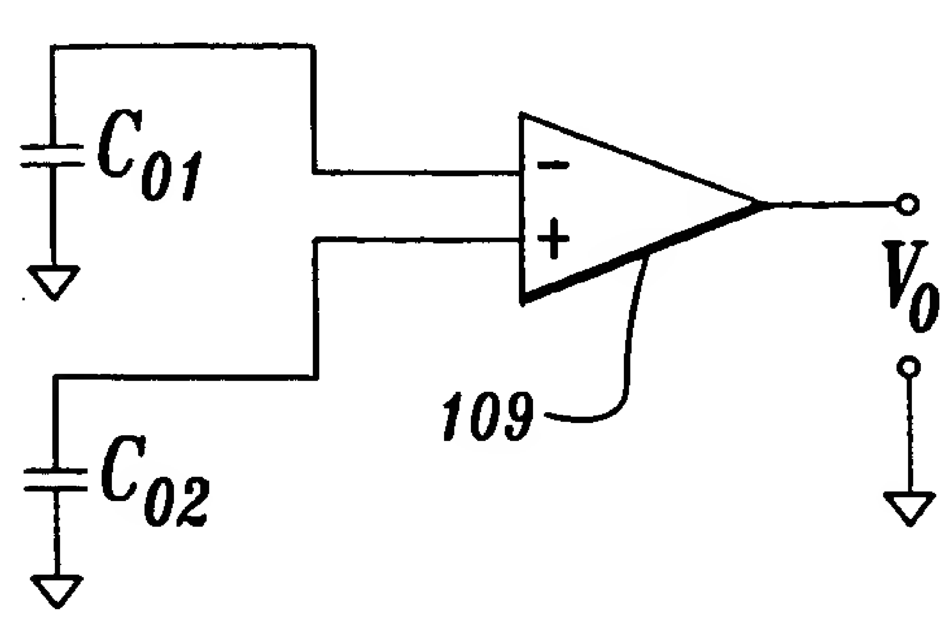


Fig. 5



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/20218

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H04N 5/335
US CL :348/301, 302

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 348/301, 302, 294, 300, 307, 308; 250/208.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS
Search terms: MOS, refernce voltage, shield?, amplified or amplifying

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category°	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,448,056 A (TSURUTA) 05 September 1995, col. 4, lines 33-68.	1-11
A	US 4,439,693 A (LUCAS ET AL) 27 March 1984, col. 3 and col. 4.	1-11
A	US 4,577,230 A (OZAWA ET AL) 18 March 1986, col. 5, lines 51-68 and col. 6, lines 1-41.	1-11
A	US 5,473,660 A (BASTIAENS ET AL) 05 December 1995, col. 4, lines 17-68 and col. 5, lines 1-8.	1-11

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

° Special categories of cited documents:

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search

22 JANUARY 1998

Date of mailing of the international search report

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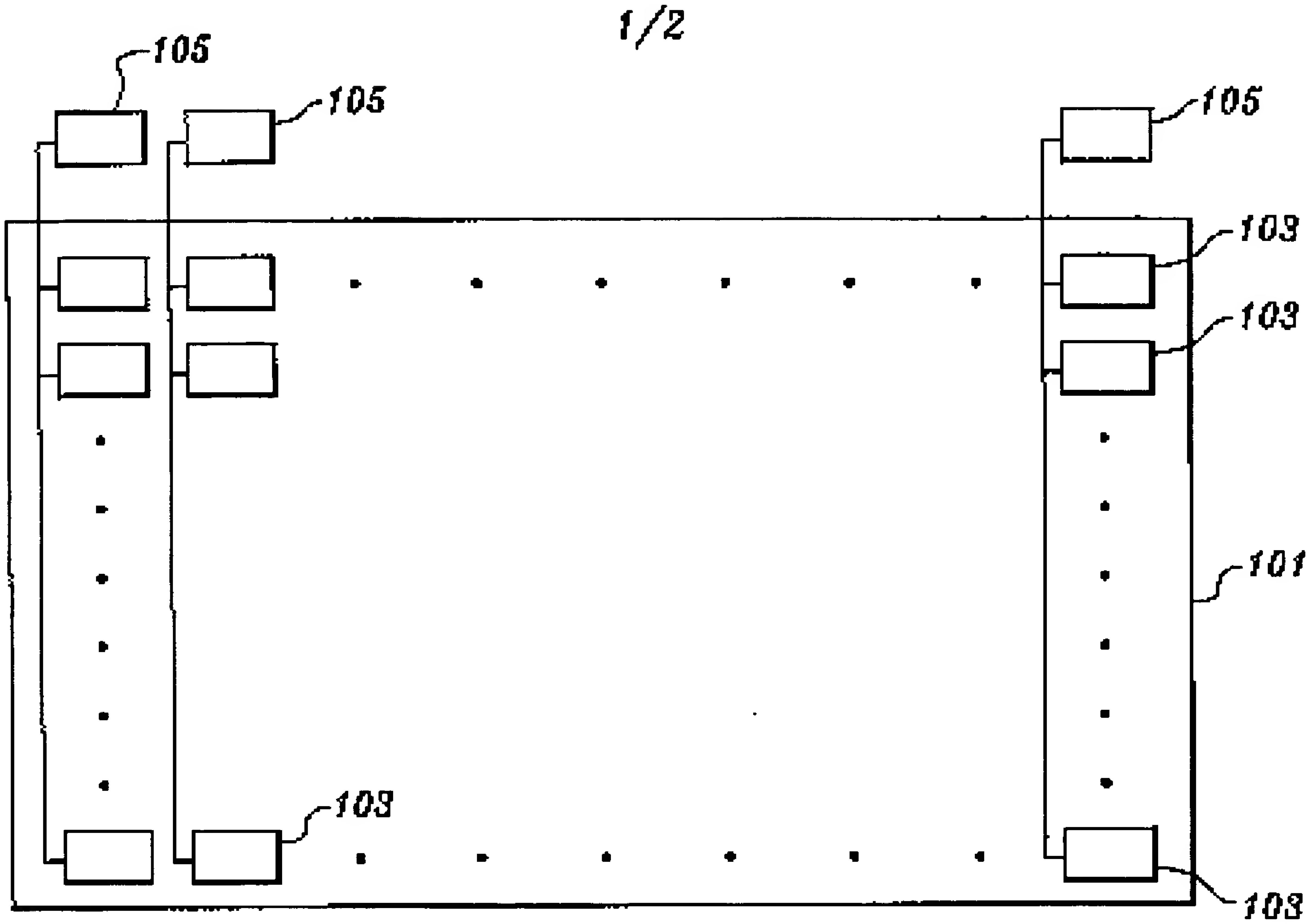
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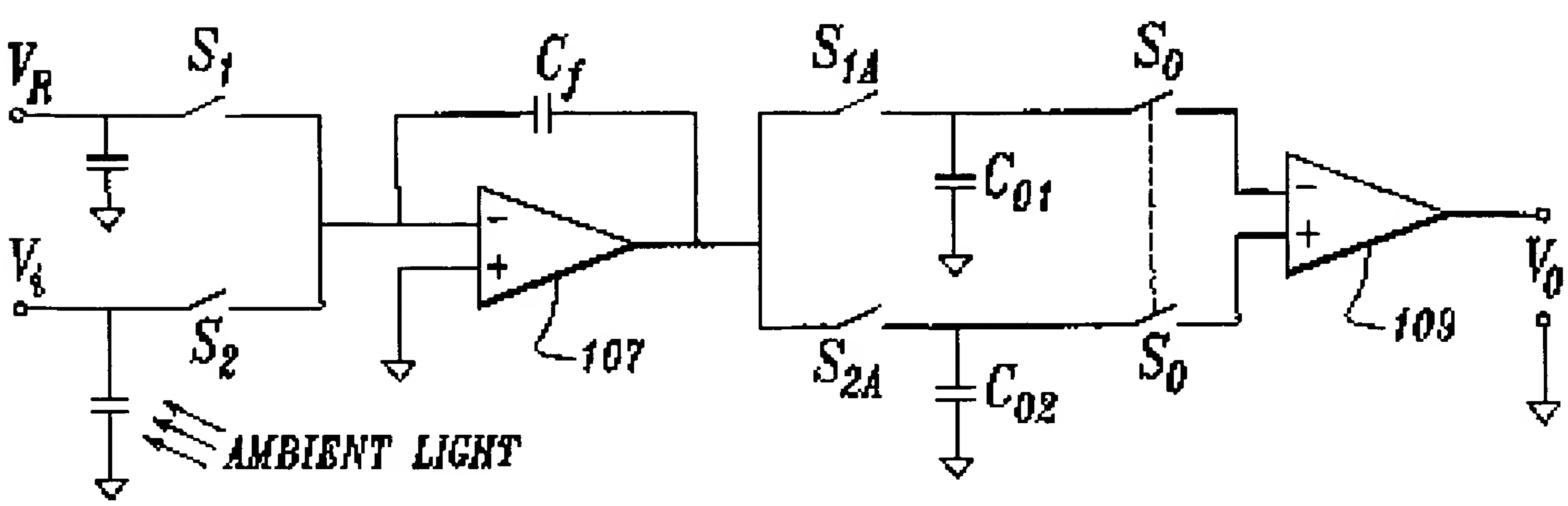
Fig. 1A


V_R
S_1
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C_{01}
V_i
S_2
107
S_{2A}
C_{02}
S_0
109
V_0
AMBIENT LIGHT

Fig. 1B

Fig. 2A

Fig. 2B

Fig. 2C

Fig. 2D

Fig. 2E

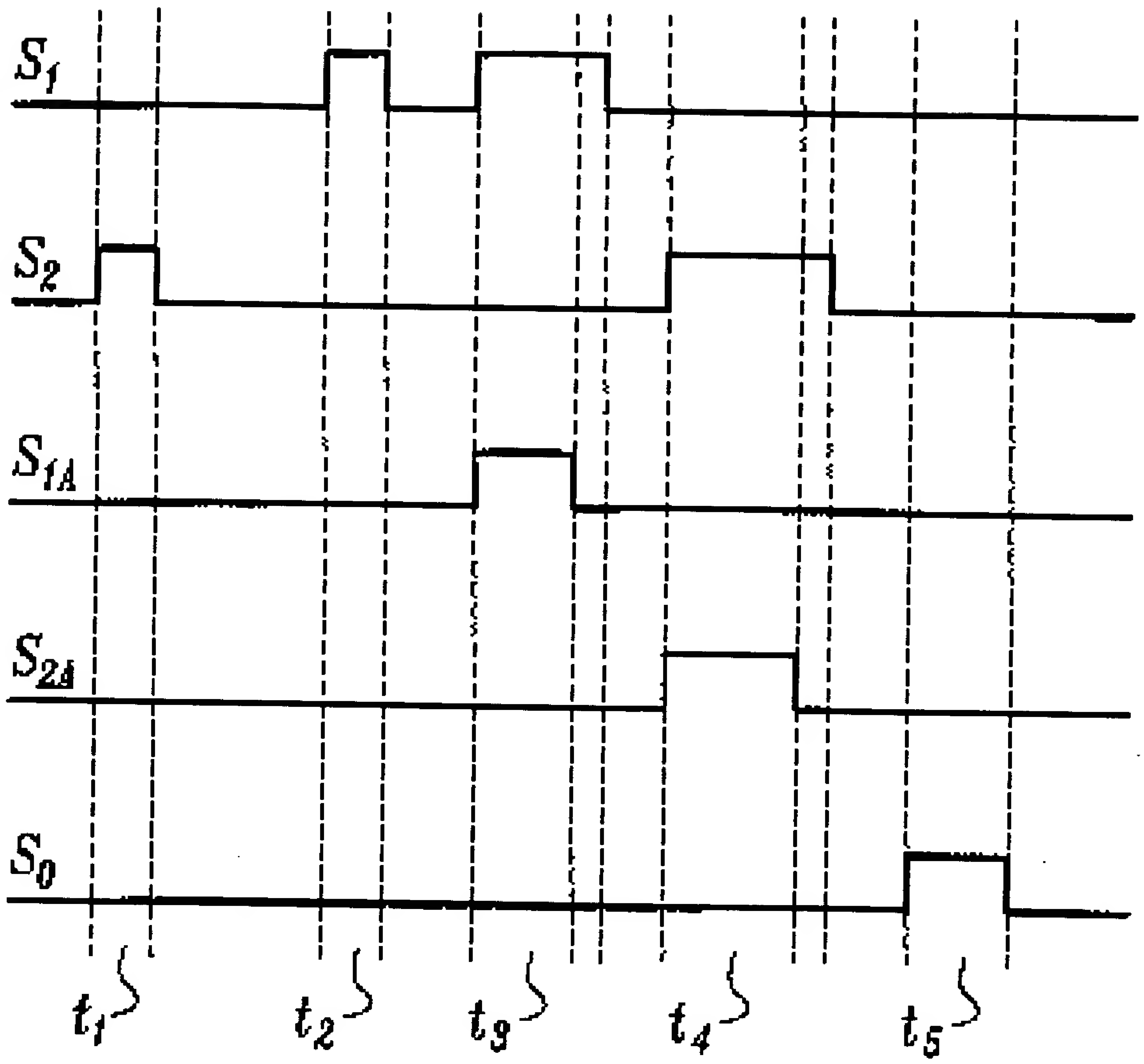

Fig. 3

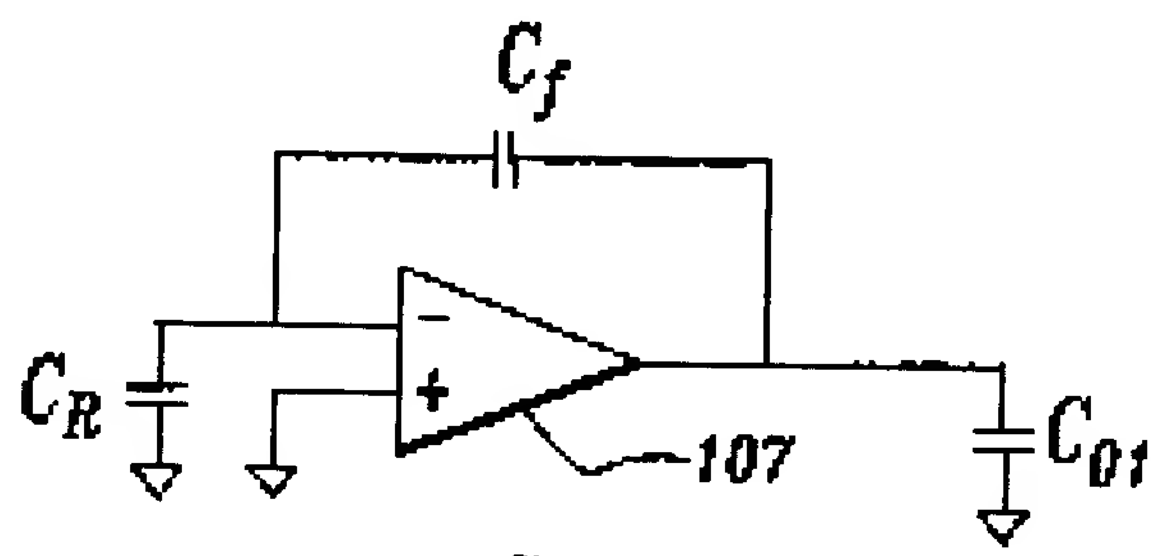

Fig. 4

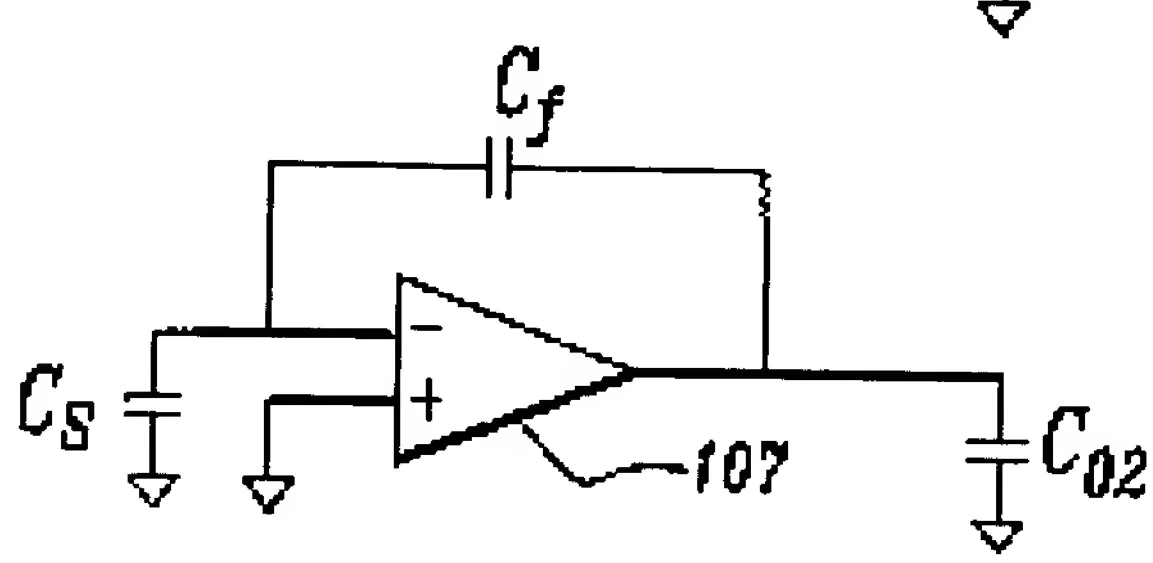

Fig. 5